



Docket No.: 1081.1102

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Masatoshi AKAGAWA

Serial No. 09/754,323

Group Art Unit: 2823

Confirmation No. 3680

Filed: January 5, 2001

Examiner: Scott A. Brairton

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

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**LETTER TO THE EXAMINER REQUESTING
APPROVAL OF THE CHANGES TO THE DRAWINGS**

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

It is respectfully requested that the Examiner having jurisdiction over the subject application approve the amendments to the drawings as indicated in RED on the attached copy of Figures 1A-D.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Sept 18, 2002

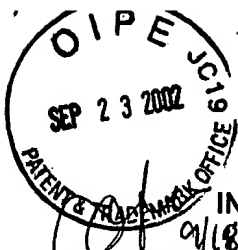
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CERTIFICATE UNDER 37 CFR 1.8(a)

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on September 18, 2002
By: Patricia M. Halsey
Date: September 18, 2002



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AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

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on September 18, 2002

STAAS & WALSEY

By: [Signature]

Date: September 18, 2002

Sir:

This is in response to the Office Action mailed June 18, 2002, and having a period for response set to expire on September 18, 2002.

The following amendments and remarks are respectfully submitted. Reconsideration of the claims is respectfully requested.

IN THE CLAIMS:

Please AMEND the following claims:

1. (ONCE AMENDED) A semiconductor device comprising: ^{22, 24} plural pairs of conductor layers having wiring patterns and an insulating layer located thereon; wherein: ³⁰
- a semiconductor element is imbedded inside said insulating layer;
- the semiconductor element is electrically connected to a wiring pattern of said conductor layer; and
- a wiring pattern of said conductor layer is electrically connected, by via holes ^{VH1, VH2}, to a wiring pattern of the conductor layer of a different pair of a conductor layer having wiring patterns and an insulating layer located thereon.

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